Experiment Report

D-Flip Flop Design

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## Aim

74LS74 is ascending edge trigger D flip-flop (from 1 to zero). 74LS74 has two internal D flip-flops. The truth table of 74LS74 can be found in the system.

1. Test and fill in the truth table of D flip-flop
2. Use D flip-flop build counter
3. Use logic analyzer to observe the counter waveform

## Content and steps

1. Use a single 74LS74 chip for circuit connection as required

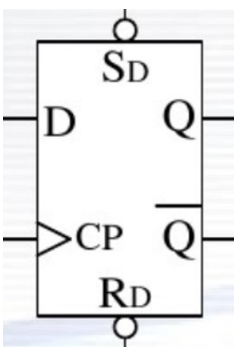
2. Use the single pulse output area of the operation box to simulate the system clock and measure the truth table of the D flip-flop.

3. Connect the Base4 Counter circuit according to the drawing

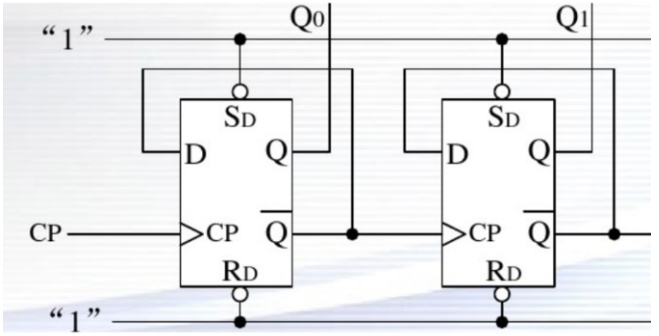
4. Analyze the counting principle of the circuit using the logic analyzer area

## Circuit

Experiment 1：



Experiment 2:



## Analysis

74LS74 is an integrated circuit commonly used in digital logic circuits. It is a component called a 'D Flip Flop'. To design a counter, you can use the 74LS74 chip as one of the basic components for building counting logic.

Firstly, analyze the truth table.

Sd 'and Rd' can directly control the output of Q and Q '. When Sd'=0 and Rd '=1, regardless of Qn, the output of Q (n+1) must be 1; When Sd '=1 and Rd'=0, regardless of Qn, the output of Q (n+1) must be 0; When Sd '=Rd'=1, the output of Q remains unchanged; But when Sd '=Rd'=0, this is an illegal state.

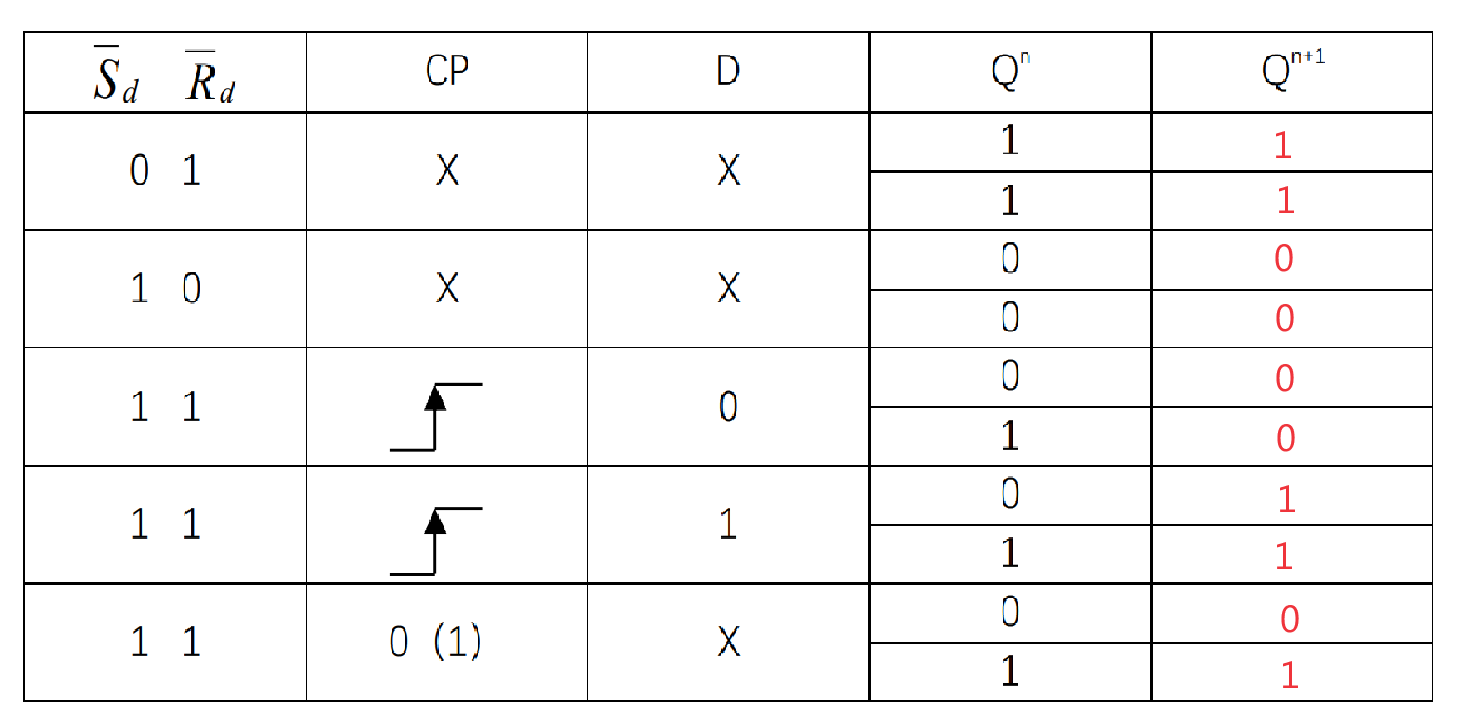
Now we will focus on the case where Sd '=Rd'=1. In this case, D serves as the signal that is about to be written, and CP can control whether D is allowed to be written. When CP is on its upper edge, signal D is written, and the state of Q (n+1) becomes D.

Then, analyze the counter.

This counter consists of two D latches, whose inputs are controlled by CP. In this circuit, Q0 and Q1 are the output terminals, while Q0 'and Q1' are reversed to D0 and D1, forming a set of asynchronous registers where the write times of the two latches are not at the same time. Through CP input, the first latch is written at the time of its upper jump, and then through asynchronous register operation, the second latch is written at the time of its lower jump. In this way, different cycles are formed for each latch, thereby forming a counter

## Result

In the experiment we get the truth table of D filp-flop,



As shown in the figure, it is the circuit connection diagram for this experiment. The counter results obtained by the logic analyzer are displayed on the electronic screen in the lower right corner of the test box. The third line of signals displays the original CP cycle. After observation, it is not difficult to find that the second line of signals (corresponding to the first latch) only changes at the upper edge of the CP, and the first line of signals (corresponding to the second latch) only changes at the lower edge of the first latch. This is consistent with our previous analysis. Prove the success of our experiment.

